An improved But Reliable Model for MESFET Parasitic Capacitance Extraction

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Abstract-- The conventional parasitic capacitance extraction always produces bias-dependent C_{pd}, even though from the underlying physic, the parasitic capacitance is known to be bias-independent. In this paper, an improved model is thus proposed to evaluate the parasitic capacitances of GaAs MESFET transistor from the cold-FET S-parameters measurement. The resulting C_{pd} is found to be independent of V_{gs} when $V_{gs}<V_p$. In our approach, model parameters can be uniquely determined by using only two sets of cold-FET S-parameters under different V_{gs} biasing condition.

Index Terms--Small Signal Equivalent Circuit

I. Introduction

The small signal equivalent circuit of MESFET is very useful for device performance analysis and microwave circuit design. A typical small signal equivalent circuit of the microwave MESFET is shown in Fig. 1. It consists of the intrinsic elements, which are enclosed by the dashed-box as shown in Fig. 1, and the extrinsic parasitic elements, which include the element R_s, R_g, R_d, L_s, L_g L_d, C_{pg} and C_{pd}. The intrinsic components are usually calculated after a de-embedding process through which the effect of the parasitics is removed. As such, it becomes very crucial that all external parasitics be accurately determined.

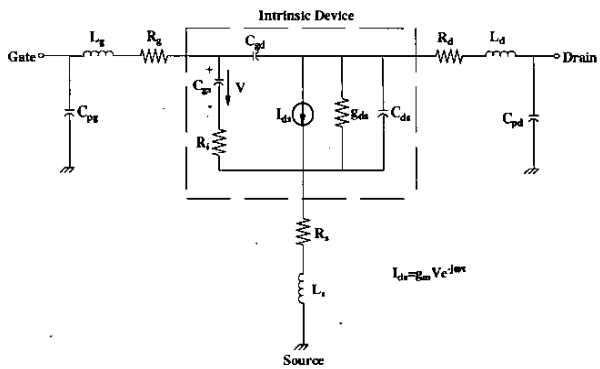

Fig. 1. MESFET small-signal equivalent circuit

The determination of the parasitic capacitances is always based on the measured Y-parameters at the gate bias beyond the pinch-off voltage ($V_{gs}<V_p$), and with both the source and the drain grounded ($V_{ds}=0$). Fig. 2 shows the Y-parameters of a 2*150μm MESFET device. As noted from the figure, when the frequency is low, the influence of the parasitic resistances and inductances on the imaginary parts of the Y-parameters, $\mathrm{Im}(Y_{ij})$, can be neglected. The imaginary parts of the Y parameters can be taken to be caused by the capacitive effect. Based on this assumption, two models are commonly used for estimating C_{pg} and C_{pd} [1] & [2].

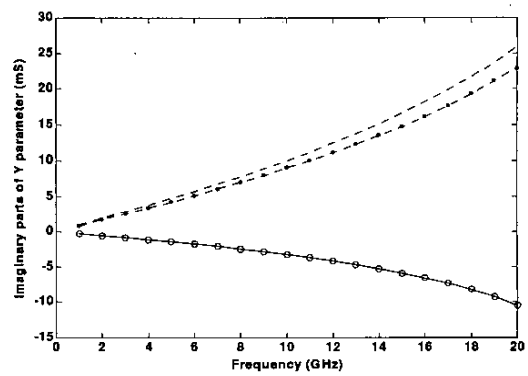

Fig. 2. Imaginary parts of Y parameters versus frequency. Measured at $V_{ds}=0$, $V_{gs}=-5.0$, $V_{gs}<V_p$, 0.5μm, 2*150μm MESFET (---- Y_{11}, —— Y_{12}, ooo Y_{21}, --●-- Y_{22})

II. Dambrine's Model[1]

The equivalent circuit of the Dambrine's model is shown in Fig. 3. The model assumes that under cold-FET condition with V_{gs} biased at pinch-off region, the depletion region beneath the gate can be modeled by two capacitors with the same value, C_b, which is the fringing capacitance due to depletion layer extension at each side of the gate. At low frequency, the imaginary parts of the Y parameter can thus be written as:

$$\mathrm{Im}(Y_{11}) = j\omega(C_{pg} + 2\cdot C_b), \quad (1)$$

$$\mathrm{Im}(Y_{12}) = \mathrm{Im}(Y_{21}) = -j\omega C_b, \text{ and} \quad (2)$$

$$\mathrm{Im}(Y_{22}) = j\omega(C_b + C_{pd}). \quad (3)$$

Hence, the elements C_{pg} and C_{pd} can be extracted from

$$C_{pg} = \frac{\mathrm{Im}(Y_{11}) + 2\,\mathrm{Im}(Y_{12})}{\omega}, \text{ and} \quad (4)$$

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$$C_{pd} = \frac{\mathrm{Im}(Y_{22}) + \mathrm{Im}(Y_{12})}{\omega}. \quad (5)$$

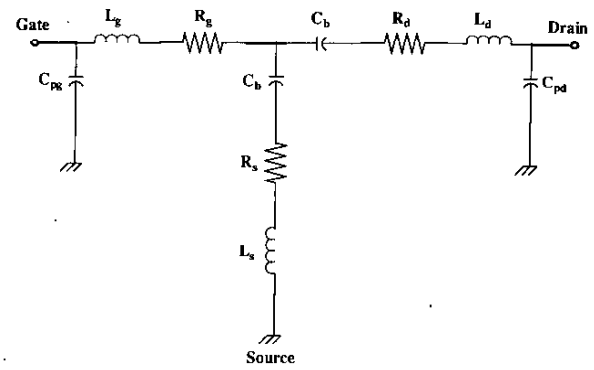


Fig. 3. Small-signal equivalent circuit at V_{ds}=0 and V_{gs}<V_p for Dambrine's model.

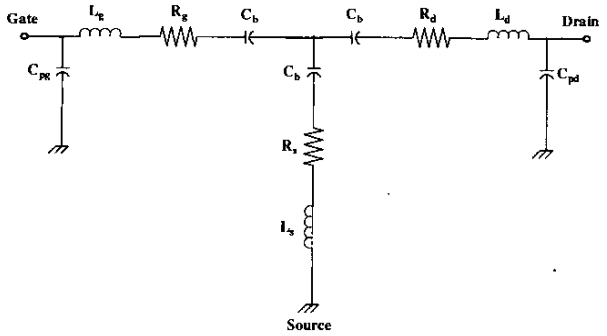


Fig. 4 White's small-signal equivalent circuit model at V_{ds}=0 and V_{gs}<V_p.

III. White's Model [2]

The equivalent circuit of the White's model is shown in Fig. 4. The depletion region under the gate is modeled by three re-defined identical capacitors C_b, connecting to gate, source and drain respectively. The connecting node can be explained as a hypothetic point within the depletion region. It is positioned in such a way so that the capacitances with respect to the gate, the drain and the source are all equal. When frequency is low, the imaginary parts of the Y parameter can be written as:

$$\mathrm{Im}(Y_{11}) = j\omega(C_{pg} + \frac{2}{3}C_b), \quad (6)$$

$$\mathrm{Im}(Y_{12}) = \mathrm{Im}(Y_{21}) = -j\omega\frac{C_b}{3}, \text{ and} \quad (7)$$

$$\mathrm{Im}(Y_{22}) = j\omega(2\cdot C_b + \frac{2}{3}C_{pd}). \quad (8)$$

The capacitances C_{pg} and C_{pd} are determined from

$$C_{pg} = \frac{\mathrm{Im}(Y_{11}) + 2\,\mathrm{Im}(Y_{12})}{\omega}, \text{ and} \quad (9)$$

$$C_{pd} = \frac{\mathrm{Im}(Y_{22}) + 2\,\mathrm{Im}(Y_{12})}{\omega}. \quad (10)$$

As noted from the above equations, both models yield the same results for the parasitic capacitance C_{pg}. However, different expressions are obtained for the capacitance C_{pd} under the two models.

To study the problem in greater detail, the cold FET S-parameters are measured for a 2*100μm and a 2*150μm MESFET devices. For both devices, the measurements are made under three different V_{gs} bias points, all beyond pinch-off, with V_{ds}=0. Parasitic capacitances C_{pg} and C_{pd} are computed using these measured data for both the Dambrine's and White's Model. The result is depicted in Fig. 9.

As observed from Fig. 9, the extracted C_{pg} remains relatively constant under different V_{gs} bias condition (all beyond pinch-off) for both Dambrine's and White's model. Both transistors give similar trend for the extracted C_{pg}. This result is in agreement with the bias independent nature of the parasitic capacitance C_{pg}.

From Fig. 9, it is also noted that the extracted C_{pd} under different bias conditions varies widely for the two models. As seen from the figure, the White's model has the largest variation in the extracted C_{pd} as compared to the Dambrine's model. Both transistors show similar trend for the extracted C_{pd}. The extracted C_{pd} values from both models are in violation with the bias independent nature of the parasitic capacitance. Thus, a more accurate and reliable extraction technique for the capacitance C_{pd} is needed.

IV. The Proposed Model

Fig. 5 shows the equivalent circuit of our improved model for MESFET biasing at V_{gs}<V_p and V_{ds}=0. The depletion region under the gate is modeled by three Π capacitors, connected from the gate to the source C_f, from the gate to the drain C_f, and between drain and source αC_f. The proposed model can be transformed into a TEE topology and this is depicted in Fig. 6. The physical origin of the new model elements is illustrated in Fig. 7, in which the depletion region is described by three capacitances associated with gate, drain and source. The connecting point P can be taken as a hypothetic node within the depletion region. An additional parameter α is introduced to adjust the location of P such that the capacitances from P to gate, source and drain are $(2+1/\alpha)C_f$, $2(2+1/\alpha)C_f$ and $2(2+1/\alpha)C_f$ respectively. It can be seen that the capacitances from P to drain and source are the same, while the capacitance from P to gate has a different value.

When frequency is low, the imaginary parts of the Y parameters can be written as:

$$\mathrm{Im}(Y_{11}) = j\omega(C_{pg} + 2\cdot C_f), \quad (11)$$

$$\mathrm{Im}(Y_{12}) = \mathrm{Im}(Y_{21}) = -j\omega C_f, \text{ and} \quad (12)$$

$$\mathrm{Im}(Y_{22}) = j\omega(C_{pd} + C_f + \alpha C_f). \quad (13)$$

Hence, both C_{pg} and C_{pd} can be determined from

$$C_{pg} = \frac{\mathrm{Im}(Y_{11}) + 2\,\mathrm{Im}(Y_{12})}{\omega}, \text{ and} \quad (14)$$

$$C_{pd} = \frac{\mathrm{Im}(Y_{22}) + (1+\alpha)\,\mathrm{Im}(Y_{12})}{\omega}. \quad (15)$$

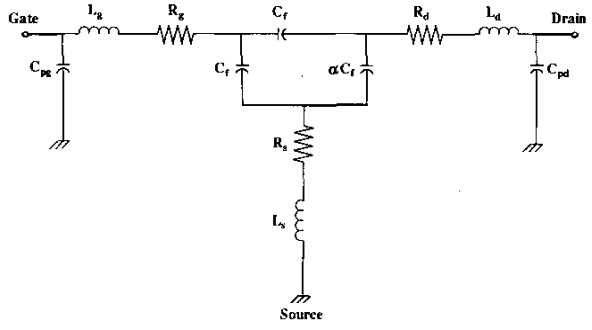


Fig. 5. Equivalent circuit of the improved model for MESFET biasing at $V_{gs}<V_p$ and $V_{ds}=0$, intrinsic elements in Π topology

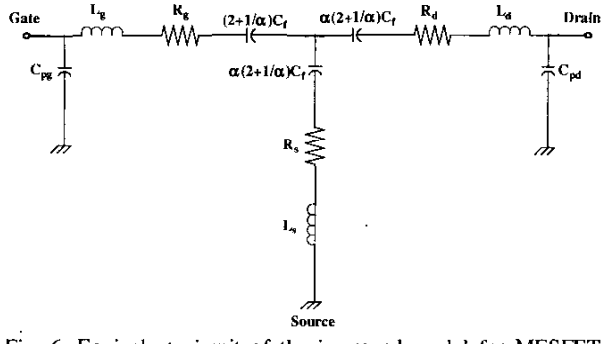


Fig. 6. Equivalent circuit of the improved model for MESFET biasing at $V_{gs}<V_p$ and $V_{ds}=0$, intrinsic elements in TEE topology

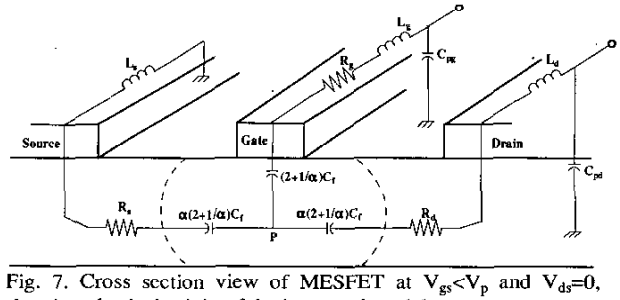


Fig. 7. Cross section view of MESFET at $V_{gs}<V_p$ and $V_{ds}=0$, showing physical origin of the improved model

The parameter α in equations (13) and (15) is an additional parameter for modeling, and it can be determined through the procedures described below.

Assuming YA is the Y-parameter from the cold-FET measurements for $V_{gs}=V_{gs1}<V_p$, and $V_{ds}=0$, YB is the Y-parameter from cold-FET measurement for $V_{gs}=V_{gs2}<V_p$, and $V_{ds}=0$, we have the following equations:

$$\mathrm{Im}(YA_{22}) = j\omega(C_{pd} + C_f' + \alpha C_f') = j\omega C_{pd} - (1+\alpha)\,\mathrm{Im}(YA_{12}), \quad (16)$$

$$\mathrm{Im}(YB_{22}) = j\omega(C_{pd} + C_f'' + \alpha C_f'') = j\omega C_{pd} - (1+\alpha)\,\mathrm{Im}(YB_{12}), \text{ and} \quad (17)$$

$$\alpha = \frac{\mathrm{Im}(YA_{22}) - \mathrm{Im}(YB_{22})}{\mathrm{Im}(YB_{12}) - \mathrm{Im}(YA_{12})} - 1. \quad (18)$$

Numerous experimentations have been conducted and the results show that the computed α is independent on the two V_{gs} values chosen. A typical result is shown in Fig. 8. As noted from the figure, using different cold-FET pinch-off measurement data would yield approximately the same α value.

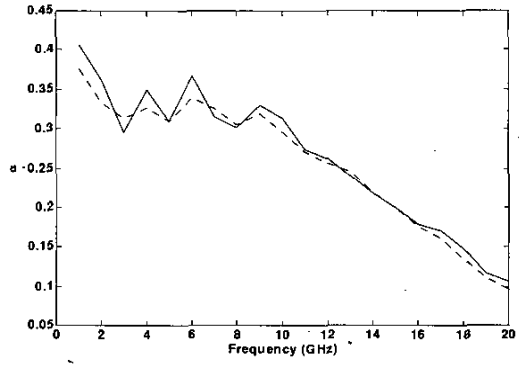


Fig. 8. Calculated α using different V_{gs} ($V_{gs}<V_p$) value, (---- α calculated with cold-FET S-parameter of V_{gs}=-5.0V and V_{gs}=-2.0V, —— α calculated with cold-FET S-parameters of V_{gs}=-5.0V and V_{gs}=-1.7V)

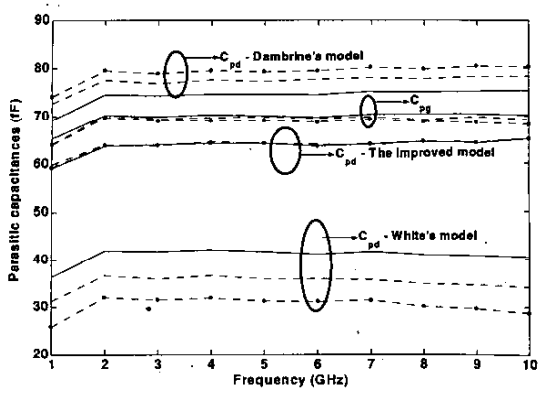
V. Verification of the Proposed Model

The same 2*100μm and 2*150μm MESFET devices are adopted for investigation. The pinch-off voltages of the devices are –1.2V and –1.23V respectively. The cold-FET S-parameters are measured under three different V_{gs} bias voltages, namely, -5.0V, -2.0V and –1.7V.

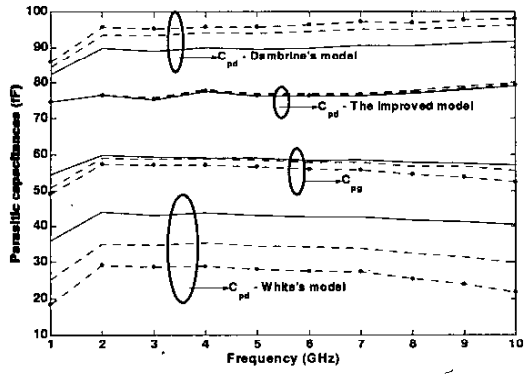
The extracted parasitic capacitances C_{pg} and C_{pd} are plotted in Figures 9(a) and 9(b). The results obtained from the Dambrine's model, and the White's models are also enclosed for comparison.

It can be seen from Fig. 9 that the calculated C_{pd} value using the improved model does not change with V_{gs}. The RMS variation of the calculated C_{pd} under the three different V_{gs} bias using Dambrine's model, White's model and the improved model is listed in Table 1. Of all the models, the proposed model has the lowest RMS variation in C_{pd}.

Based on the parasitic capacitances calculated from the improved model, the other small signal equivalent circuit parameters for the 2*100μm device are computed. A good agreement between the measured and modeled S-parameters are obtained in Fig. 10.



(a)



(b)

Fig. 9. Calculated parasitic capacitances by Dambrine's model, White's model and the improved model under three different biasing conditions (V_{ds}=0, —— V_{gs}=-5.0, ----- V_{gs}=-2.0V, --●-- V_{gs}=-1.7V), (a) 2*100μm MESFET (b) 2*150 μm MESFET.

2*100 μm			2*150 μm		
Dambrine model	White model	Proposed model	Dambrine model	White model	Proposed model
4.91%	10.6%	0.32%	6.14%	15.86%	0.67%

Table 1. The RMS variation of the calculated C_{pd} under three different V_{gs} bias conditions using Dambrine's model, White's model and the proposed model (1-10GHz).

VI. CONCLUSION

An improved and reliable model for extracting MESFET parasitic capacitance C_{pg} and C_{pd} is proposed. It is noted that the conventional parasitic extraction method gives non-physical C_{pd} value. By introducing a new capacitor in modeling the depletion region under the gate, the improved model gives accurate estimation for C_{pd}, and the result is observed to be independent of V_{gs} biasing voltage.

VII. REFERENCES

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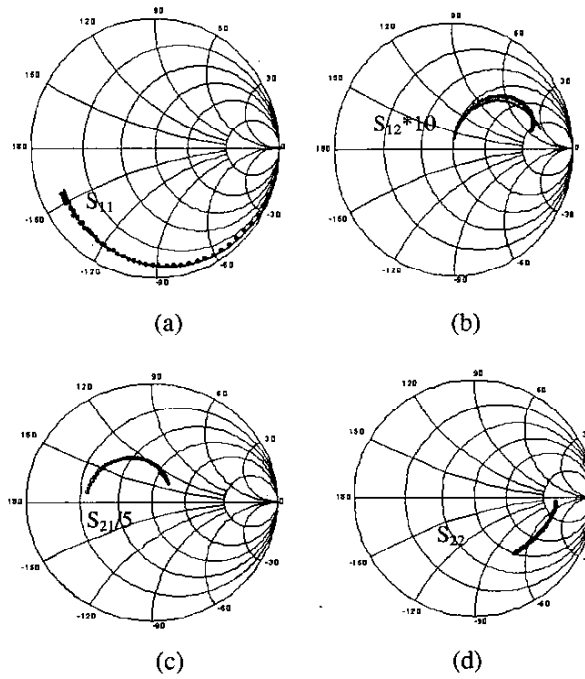

(a) (b) (c) (d)

Fig. 10. Comparison between modeled and measured S-parameter, V_{gs}=0.4V, V_{ds}=5.0V, (a) S_{11}, (b) S_{12}*10, (c) S_{21}/5, (d) S_{22}, (—— Modeled S_{11}, S_{12}, S_{21}, S_{22}, ○○○ Measured S_{11}, S_{12}, S_{21}, S_{22})